IN THE TITLE

NON-VOLATILE MEMORY AND METHOD OF FORMING THEREOF

IN THE SPECIFICATION

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Related Application

This is related to United States Patent Application Number 09/639,195 6,438,030 filed August 15, 2000, and entitled "Non-Volatile Memory, Method of Manufacture and Method of Programming" and is assigned to the current assignee hereof.

IN THE CLAIMS

- (Currently Amended and previously amended) A semiconductor device having an electrically
 erasable programmable read only memory (EEPROM) array including rows and columns
 of memory cells comprising:
 - a first well region and a second well region within a semiconductor substrate, wherein the first well region and the second well region are spaced apart and electrically isolated;
 - a first column of memory cells positioned within the first well region,;
 - a second column of memory cells positioned within the second well region;
 - a first tunnel dielectric of a first memory cell in the first column of memory cells and a second tunnel dielectric of a second memory cell in the second column of memory cells, wherein the first and second memory cells are devoid of floating gates;
 - a first charge storage layer of the first memory cell formed over the first tunnel dielectric and a second charge storage layer of the second memory cell formed over the second tunnel dielectric;
 - a first control gate of the first memory cell formed over the first charge storage layer and a second control gate of the second memory cell formed over the second charge storage layer, wherein the first control gate and the second control gate are in a same row and electrically coupled via a common wordline;